Claims

[c1]   1. A method of transferring a large volume of data from a source memory to a destination at a desired through-put rate, said method being implemented in a memory access system, said memory access system containing a plurality of sub-systems, each of said plurality of sub-systems providing a corresponding one of a plurality of worst-case delays, said method comprising:

determining a worst case throughput rate as being in-versely proportionate to a sum of said plurality of worst-case delays;

determining a maximization factor as equaling a desired throughput rate divided by said worst case throughput rate;

providing a direct memory access (DMA) engine coupled to retrieve said large volume of data in the form of a plurality of bursts; and

providing a number of store and forward bridges (SFB) equaling one less than said maximization factor, wherein said SFBs receive said plurality of bursts and forward said plurality of bursts to said destination.

[c2]   2. The method of claim 1, wherein said SFBs are pro-

vided between said DMA and said destination.

[c3]   3. The method of claim 2, wherein one more than said number of segments are formed in a data transfer path from said source memory to said destination, said SFBs being placed such that the sub-systems contained in each of said segments provides an approximately equal aggregate maximum delay.

[c4]   4. The method of claim 3, wherein said destination comprises a destination memory.

[c5]   5. The method of claim 4, wherein each of said SFBs contains a plurality of ports for reading and writing said large volume of data in parallel.

[c6]   6. A memory access system transferring a large volume of data from a source memory to a destination at a desired throughput rate, said memory access system comprising:

a plurality of sub-systems, each of said plurality of sub-systems providing a corresponding one of a plurality of worst-case delays;

a direct memory access (DMA) engine coupled to retrieve a portion of said data in the form of a plurality of bursts; and

a number of store and forward bridges (SFB) receiving

each of said plurality of bursts and forwarding said plurality of bursts to said destination, wherein said number is determined by dividing said desired throughput rate by a worst case throughput rate, wherein said worst case throughput rate is inversely proportional to a sum of said plurality of worst-case delays.

[c7]   7. The memory access system of claim 6, wherein said SFBs are provided between said DMA and said destination.

[c8]   8. The memory access system of claim 7, wherein one more than said number of segments are formed in a data transfer path from said source memory to said destination, said SFBs being placed such that the sub-systems contained in each of said segments provides an approximately equal aggregate maximum delay.

[c9]   9. The memory access system of claim 8, wherein said destination comprises a destination memory.

[c10]   10. The memory access system of claim 9, wherein each of said SFBs contains a plurality of ports for reading and writing said large volume of data in parallel.

[c11]   11. The memory access system of claim 7, wherein said number equals 1.

[c12]   12. The memory access system of claim 7, wherein said plurality of sub-systems and said destination memory are contained in a system-on-a-chip, and wherein said source memory is located external to said system-on-a-chip.

[c13]   13. The memory access system of claim 12, wherein said plurality of data bursts comprise a plurality of software instructions which are to be executed by a processor contained in said system-on-a-chip.

[c14]   14. The memory access system of claim 7, wherein each of said SFB comprises:
an inport interface receiving a first burst of data and an address at which to store said first burst of data;
a data FIFO storing said first burst of data;
a control FIFO storing said address;
an outport interface;
a control block transferring said first burst of data on said outport interface to said destination.

[c15]   15. The memory access system of claim 14, wherein said control block sends an acknowledgment on said inport interface upon storing said first burst of data and said address.

[c16]   16. The memory access system of claim 14, wherein said

control block receives an acknowledgment after transferring said first burst of data, and removes said first burst of data from said data FIFO and said address from said control FIFO in response to receiving said acknowledgment.